XXth International Workshop on Physics of Semiconductor Devices: IWPSD 2019

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Tutorial 3:

Title: Towards the end of Moore's Law: Options and Challenges Beyond Advanced FinFET Technologies to Sustain CMOS ULSI

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Abstract:

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1. The Short Channel Effects: Threshold voltage change with channel length scaling, Drain Induced Barrier Lowering, Channel Length Modulation, Velocity Saturation, Mobility Degradation, Punch-through, HC effects, parasitic bipolar effect, Gate Induced Drain Leakage, Effect of thin Gox, Transistor Scaling and scaling Implications.

2. Double Gate MOSFET and FinFETs: FDSOI and PDSOI. Limitation of FDSOI technology.Why FinFETs? FinFET advantages over FDSOI, FinFET Design, SOI vs. Bulk FinFETs, band diagram, scaling and variability issues/advantages, effect of Fin Width, effect of S/D resistance, mobility, quantum confinement effects and bulk conduction. P and N conduction, impact of crystal plane. High-k & Metal Gate for FinFETs, Process flow and complexities, doping thin films, raised S/D, epitaxial S/D, stress and other mobility boosters. FinFET based circuit design advantages (Logic, SRAM, Analog/RF), limitations and other challenges. FinFET layout design rules. HV/ESD device and SoC design challenges in FinFETs. Nanowire FETs – Challenges and Opportunities. Tunnel FETs – Challenges and Opportunities.

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